

# Dicing of APV Readout Chips for FGT & IST

Gerrit van Nieuwenhuizen  
FGT meeting  
BNL, February 27, 2009

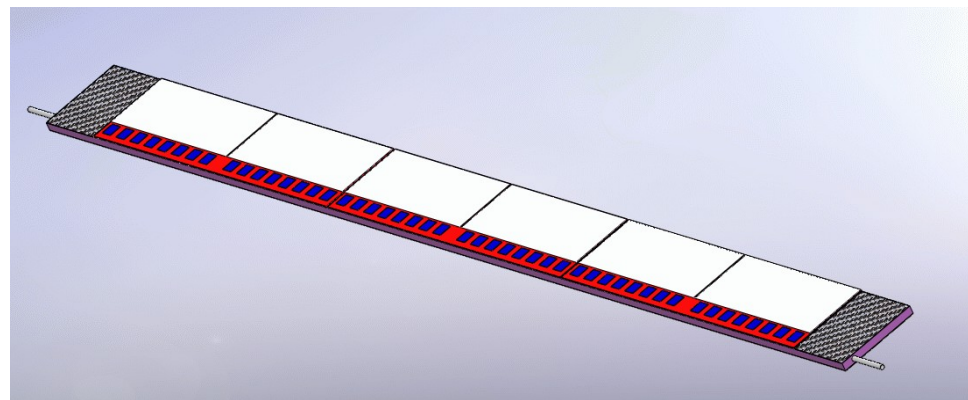
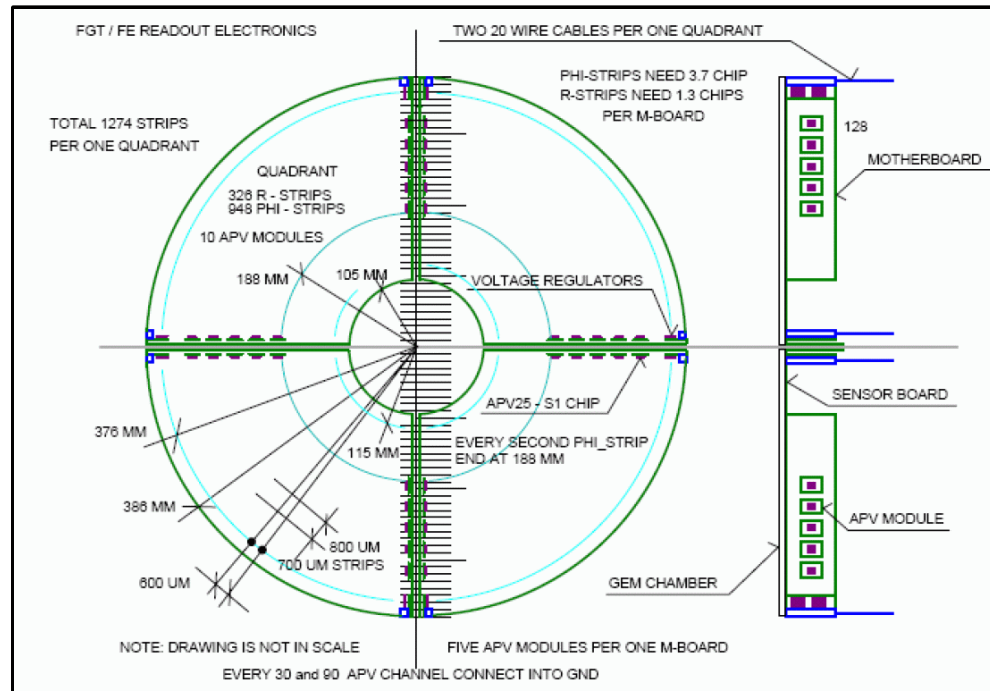
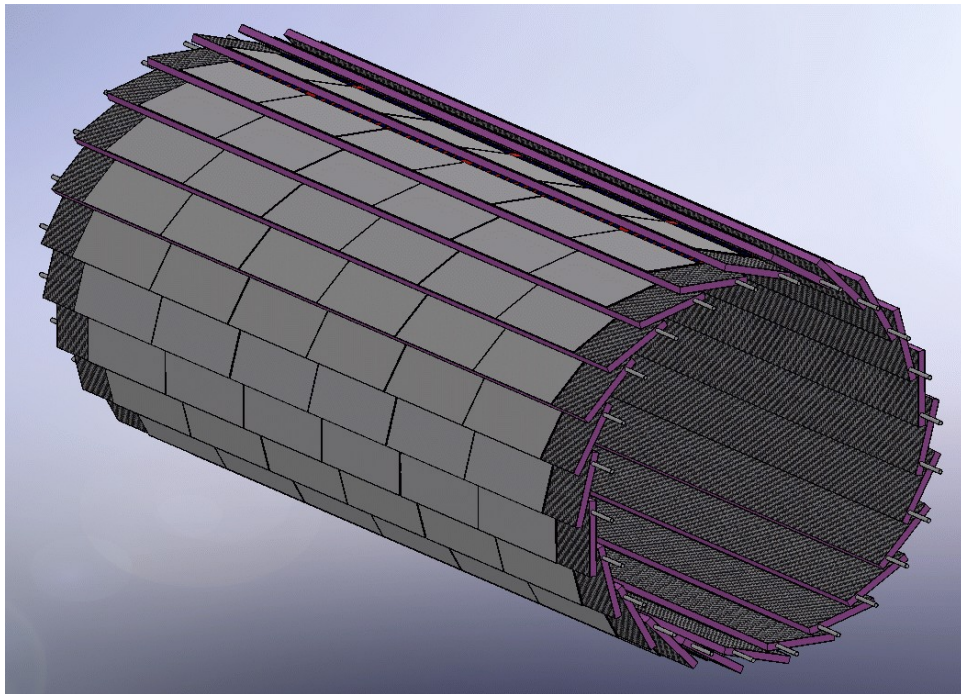


**The STAR experiment**

at the Relativistic Heavy Ion Collider, Brookhaven National Laboratory



# Number of chips needed



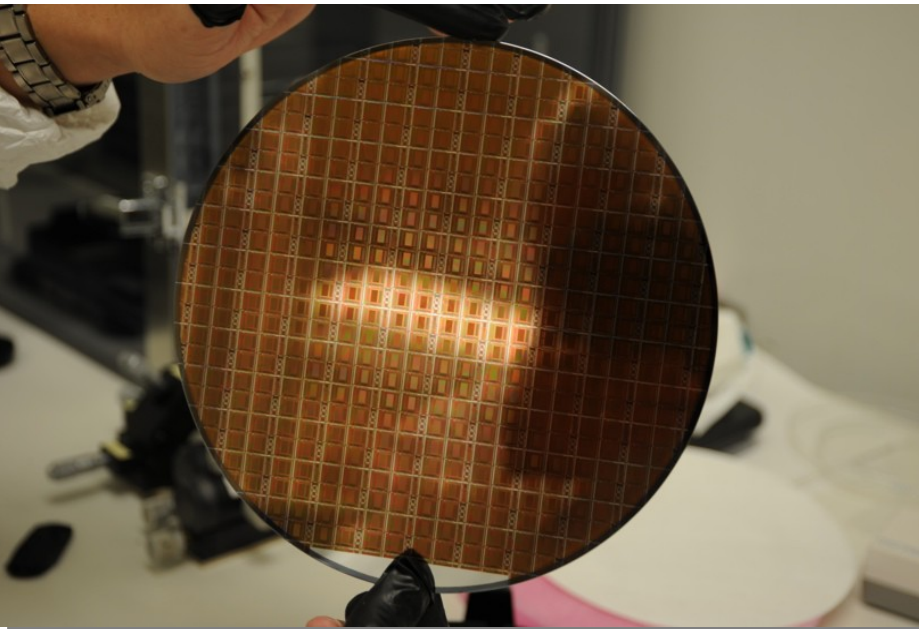
**FGT: 600 chips (50% spares, 40% cont.)**

**IST: 1800 chips (10% spares, 40% cont.)**

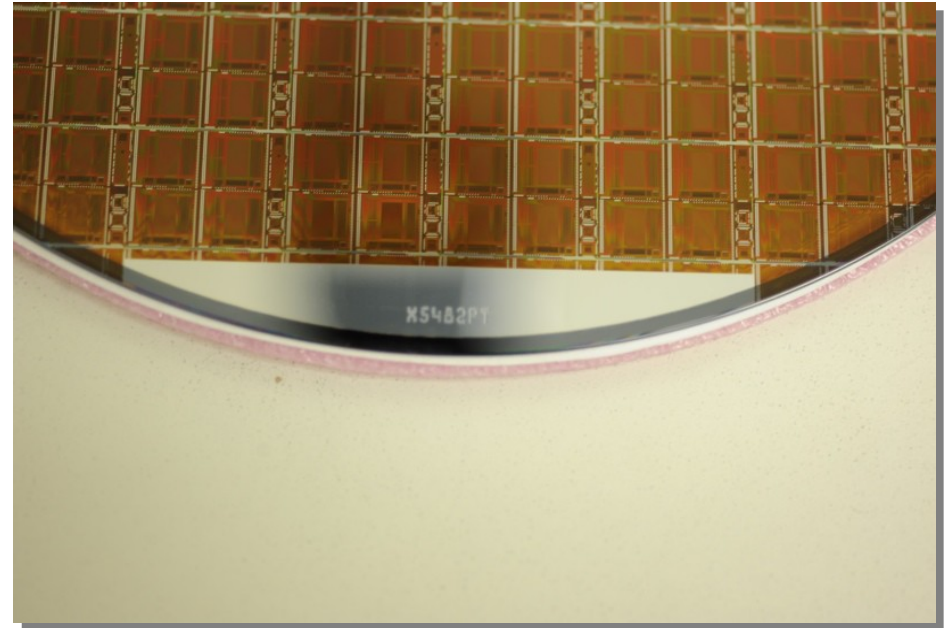
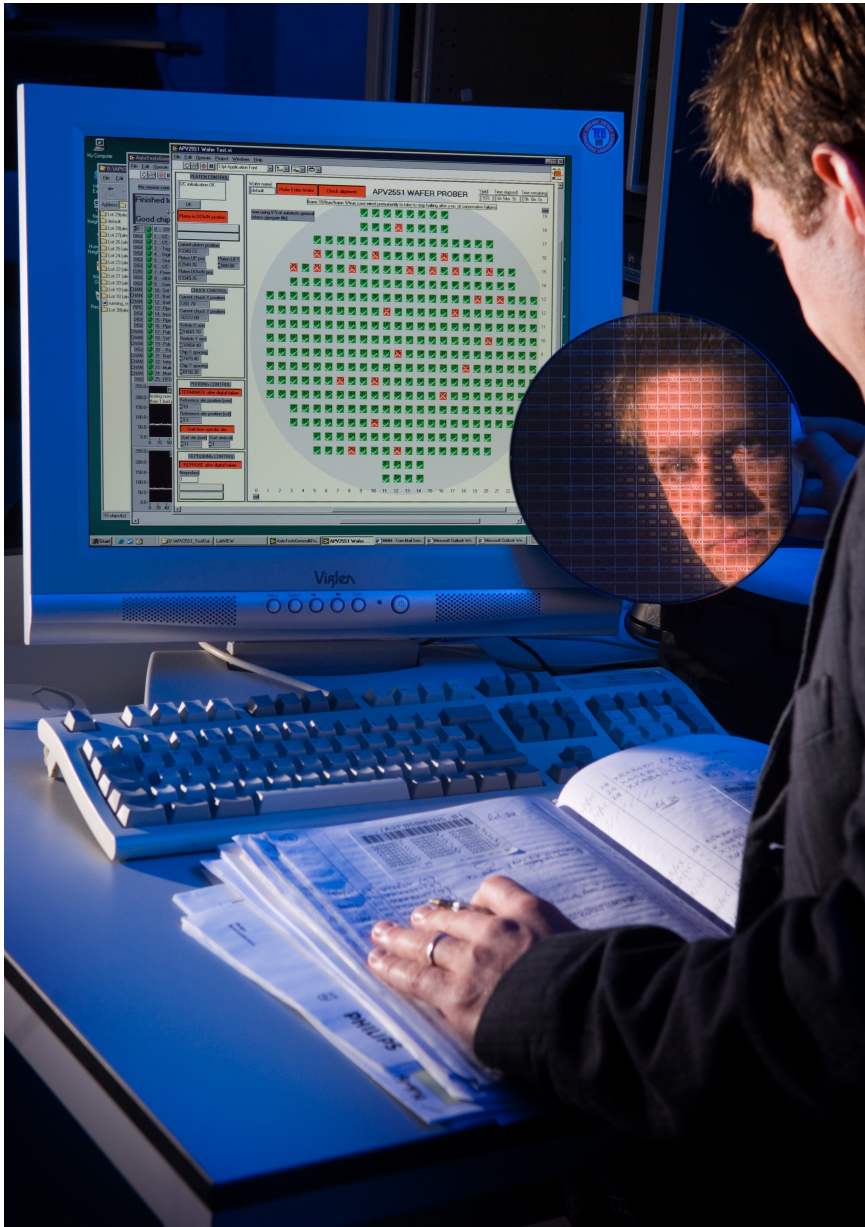
**2400 APV25-S1 chips to procure**



# 8 APV Wafers at MIT



# How many good chips?



**Each wafer has its ID etched in**

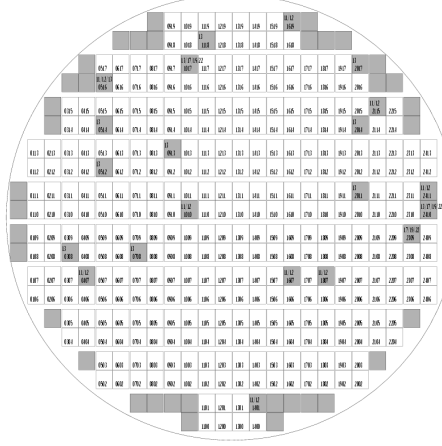
**All chips on the wafers were probed for functionality**

**Good chip maps are available for all wafers**

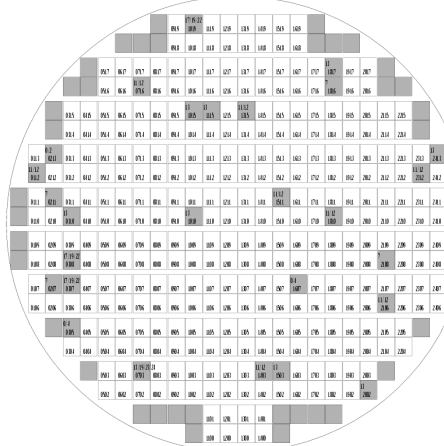


# Known Good Die (KGD) maps

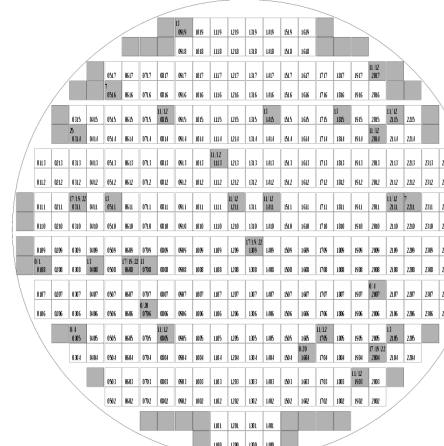
Wafer Map: K8MG5RT



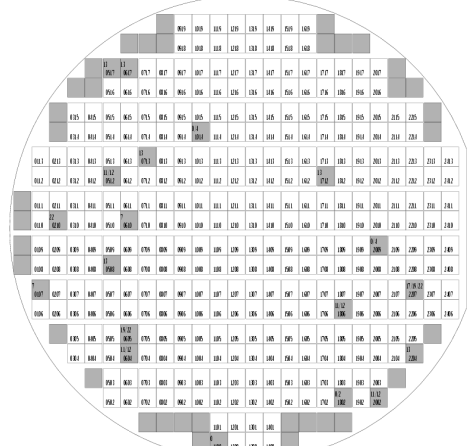
Wafer Map: X04AQYT



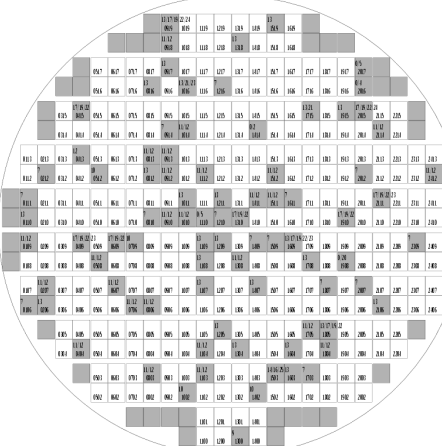
Wafer Map: X04ARFT



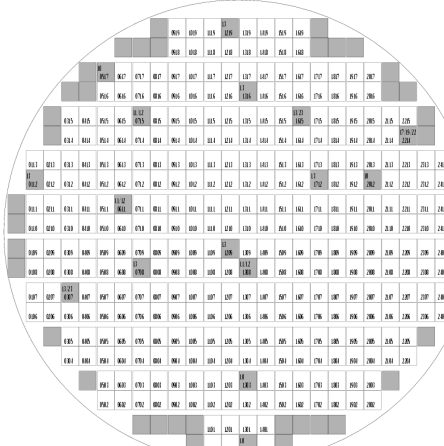
Wafer Map: X04BSWT



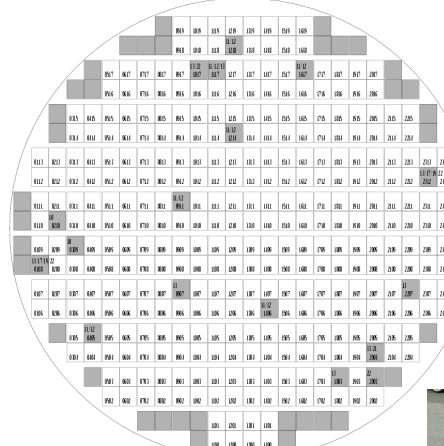
Wafer Map: X14AQXT



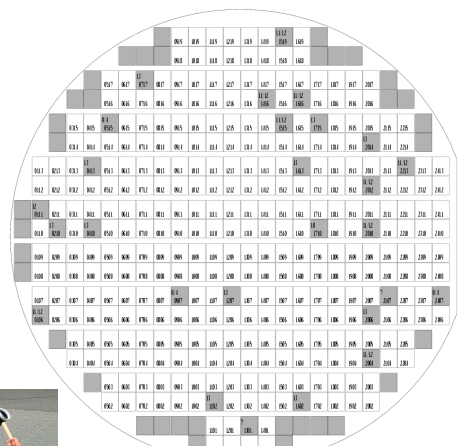
Wafer Map: X14ARET



Wafer Map: X5482PT



Wafer Map: X6482NT



And the final tally is.....

.....

# Number of good APV25-S1 chips

Dear all,

8 APV wafers are on their way to Bernd.

I would expect them to get there early next week.

The wafer identities (marked on the edges of the wafers) are:

K8MG5RT (lot 23) 339 KGD

X5482PT (lot 24) 343 KGD

X6482NT (lot 24) 333 KGD

X04ARFT (lot 29) 330 KGD

X14ARET (lot 29) 344 KGD

X14AQXT (lot 29) 274 KGD

X04AQYT (lot 29) 333 KGD

X04BSWT (lot 29) 341 KGD

KGD = known good die (chips that have passed the wafer probe test)  
so there will be **2637** good chips altogether.

Wafer maps can be found on the web page  
<http://www.hep.ph.ic.ac.uk/~silicon/>  
in various formats.

Cheers, Mark.

---

Mark Raymond  
Blackett Laboratory  
Imperial College    phone: +20 7594 7799  
London SW7 2BW      fax: +20 7823 8830

---

# Dicing options



**San Jose, CA based**  
**Used with success by LBNL**



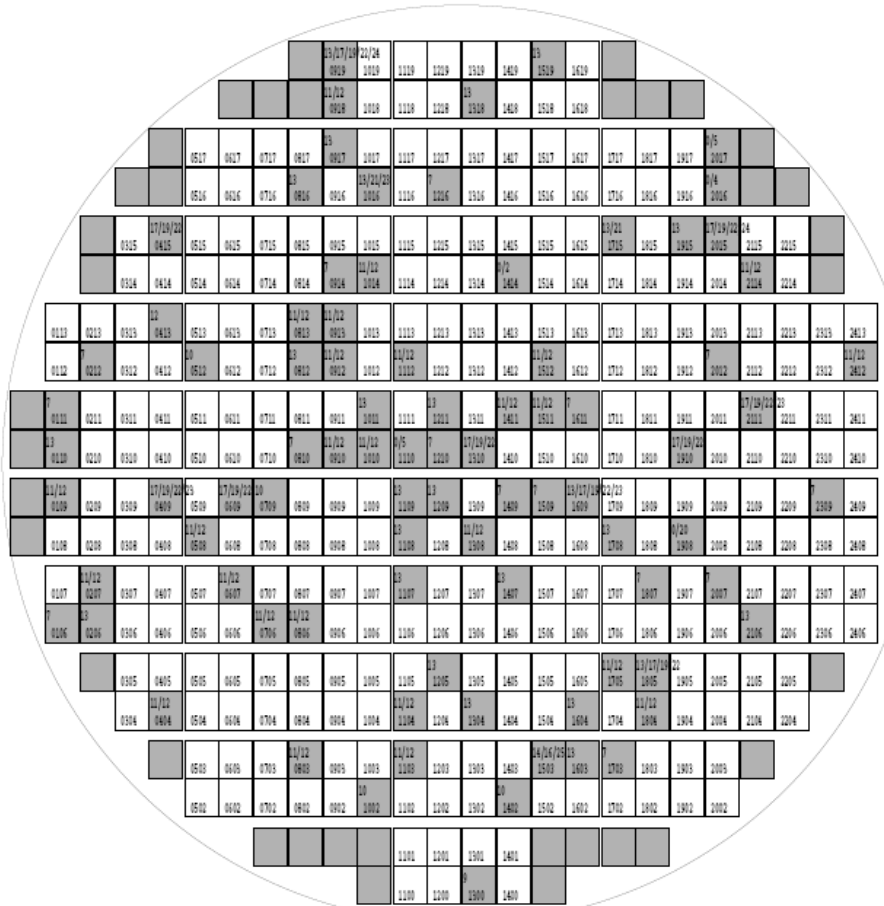
**San Jose, CA based**  
**Used with success by LBNL**



**Upton, NY based**  
**Laser dicing machine**

# Dicing information

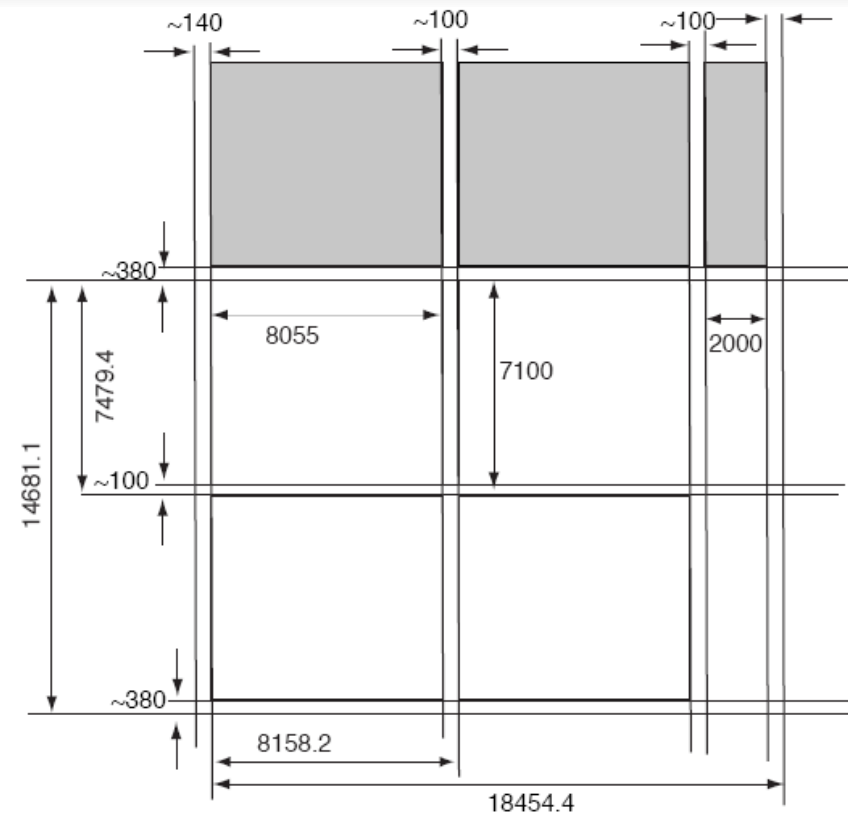
Water Map: X14AQXT



Date probed:  
Chips passed:  
Yield:

Tue 07 Jun 2005  
274/360  
76%

Digital failures: 7  
Power supply failures: 15  
Channel defects (Peds & Cal): 43  
Pipeline defects: 26



**We have the 8 wafers**  
**We have the reticle drawing**  
**Minimize the dicing cuts**  
**Get quotation.....**



# Dicing quotation



American Precision Dicing Inc.

642 Giguere Ct.  
San Jose, CA 95133  
(408) 254-1600  
www.wafer-dicing.com

Quote

Date	Quote #
2/23/2009	4628

Company

Massachusetts Institute of Technology  
Lab for Nuclear Science  
77 Massachusetts Ave.  
Cambridge, MA 021394307

Terms	Rep	FOB
C.O.D.	LI	San Jose

Item	Description	Qty	Unit Cost	Total
Dicing	Mount, Dice & Insp. Service to Dice 8" Silicon Wafer into 8.055mm x 7.1mm. Also, to include extra cuts to remove wider lanes. P/N X14ARET & APV_Reticle.	1	146.00	146.00
Jumbo Mounting ...	Jumbo Mounting Ring. (Harmonic code 844790.0000) ALL returns must be accompanied with an Invoice number. Full credit if returned within 30 days in original condition. If returned after 30 days customer will receive 25% credit. No credit if shipping hazardous materials. In house credit only.	1	9.75	9.75
Jumbo Clamshell	Jumbo Clamshell for 8" or larger wafers. (Harmonic code 844790.000) ALL returns must be accompanied with Invoice number. Full credit if returned within 30 days in original condition. If returned after 30 days customer will receive 25% credit. No credit if shipping hazardous materials. In house credit only.	1	10.75	10.75
Subtotal				\$166.50
Sales Tax (0.0%)				\$0.00
Total				\$166.50

American Precision Dicing Inc.

642 Giguere Ct.  
San Jose, CA 95133  
(408) 254-1600  
www.wafer-dicing.com

Quote

Date	Quote #
2/23/2009	4629

Company

Massachusetts Institute of Technology  
Lab for Nuclear Science  
77 Massachusetts Ave.  
Cambridge, MA 021394307

Terms	Rep	FOB
C.O.D.	LI	San Jose

Item	Description	Qty	Unit Cost	Total
Dicing	Mount, Dice & Insp. Service to Dice 8" Silicon Wafers into 8.055mm x 7.1mm. Also to include extra cuts to remove wider lanes. Wafer # X14ARET & APV_Reticle.	7	146.00	1,022.00
Jumbo Mounting ...	Jumbo Mounting Ring. (Harmonic code 844790.0000) ALL returns must be accompanied with an Invoice number. Full credit if returned within 30 days in original condition. If returned after 30 days customer will receive 25% credit. No credit if shipping hazardous materials. In house credit only.	7	9.75	68.25
Jumbo Clamshell	Jumbo Clamshell for 8" or larger wafers. (Harmonic code 844790.000) ALL returns must be accompanied with Invoice number. Full credit if returned within 30 days in original condition. If returned after 30 days customer will receive 25% credit. No credit if shipping hazardous materials. In house credit only.	7	10.75	75.25
Subtotal				\$1,165.50
Sales Tax (0.0%)				\$0.00
Total				\$1,165.50

# Dicing first wafer



**Gel-Pak®**  
Protecting the World's Valuable Devices

← Shipped to APV  
Arrived yesterday

Back diced to MIT on tape  
next week

Take off tape and store  
chips in Gel-Paks



Test some chips

# Concluding remarks

**We have 8 APV25-S1 wafers**

**These wafers should provide plenty of readout chips for both FGT and IST**

**First wafer out for dicing, back next week**

**Test some chips, if OK then dice remaining 7 wafers**